This application is a divisional of Application Serial No. 09/985,724 filed November 6, 2001, now U.S. Patent No. 6,646,907.

TITLE OF THE INVENTION

Semiconductor Memory Device

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor memory device, and particularly relates to a semiconductor memory device including memory cells, which have specific or distinctive structures, as well as a semiconductor memory device having a memory cell array, which has a specific or distinctive structure.

Description of the Background Art

A memory cell of one-transistor and one-capacitor structure is liable to loose its information, and particularly, data at a high potential level (H-data) due to leak of electric charges stored in the capacitor. In recent years, such a method has been proposed that uses two memory cells for writing H-data and L-data (i.e., data at a lower potential than H-data) therein, respectively. This method is devised to utilize a difference in amount of stored electric charges between the two memory cells, and thereby provide a Dynamic Random Access Memory (DRAM) performing a larger operation.

However, the above method requires two transistors and two capacitors, and therefore suffers from such a problem that areas of the memory cells are large. Accordingly, it has been desired to develop a semiconductor memory device, which does not occupy a large area, and can hold data with high stability.

SUMMARY OF THE INVENTION

An object of the invention is to provide a semiconductor memory device using memory cells, which have structures not increasing areas, and are arranged in a distinctive manner providing high data holding stability.

According to a first aspect of the invention, a semiconductor memory device includes memory cells formed on a main surface of a semiconductor substrate and each having first and second transistors each having a gate electrode and impurity regions forming source/drain